REMARKS

Claims 1-14, 16-18 and 21-23 are pending in the Application. Claim 1 is an independent claim and claims 2-7 and 21 depend therefrom. Claim 8 is an independent claim and claims 9-13 and 22 depend therefrom. Claim 14 is an independent claim and claims 15-18 and 23 depend therefrom. Claims 15, 19 and 20 were previously canceled. Claims 1 and 8 are currently amended. Claims 21-23 are new. The Applicant respectfully requests that the application be reconsidered in view of foregoing amendments and the following remarks.

Rejections Under 35 U.S.C. §112, First Paragraph (Claims 1-14 and 16-18)

Claims 1-14 and 16-18 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement. Specifically, the Office Action alleges that the Applicant's specification fails to disclose the "wherein the video decoding the video data is discrete from the host processor" limitation of claims 1, 8 and 14; and the "wherein the video decoder at least performs picture level processing" limitation of claims 1 and 8. The Applicant respectfully traverses the rejections for at least the following reasons.

With regard to the "wherein the video decoding the video data is discrete from the host processor" limitation of claims 1, 8 and 14, the Office Action alleges that the Applicant's specification contradicts the claim limitation. Specifically, the Office Action cites to the Applicant's Specification at Paragraph [0022], lines 4-7, which states "[t]he circuit comprises a video decoder 209, a host processor 290...." (Office Action, Page 3). The Applicant notes, however, that the cited section of the Applicant's Specification explicitly illustrates that the Applicant's video decoder 209 and host processor 290 are discrete components or modules. Note that the Applicant's Specification did **not** teach a video decoder comprising a host processor (i.e., the host processor being a part of the video decoder). Rather, the video decoder

209 and host processor are separate components or modules (i.e., the circuit comprises a separate video decoder **and** a separate host processor).

The Applicant also points to Applicant's Figure 4, which discloses an exemplary video decoder 209. The Applicant notes that nowhere in the exemplary video decoder 209 of Applicant's Figure 4 does the host processor appear. That is because the host processor is **not** part of the video decoder 209, and is instead a discrete component or module. The Applicant further notes that nowhere in the Applicant's Specification is there any mention of the Applicant's host processor performing video decoding. That is because the host processor is **not** part of the video decoder 209, and is instead a discrete component or module. Because nowhere in the Applicant's Specification is there any disclosure that the Applicant's host processor is part of the Applicant's video decoder 209 or that the host processor 290 performs video decoding, one of ordinary skill in the art would clearly understand that the Applicant's video decoder 209 and host processor 290 are discrete components or modules. Thus, the Applicant respectfully submits that the Applicant's Specification clearly supports the "wherein the video decoding the video data is discrete from the host processor" limitation of claims 1, 8 and 14, and respectfully requests that the rejections of Applicant's claims 1-14 and 16-18 under 35 U.S.C. § 112, first paragraph, be withdrawn.

With regard to the "wherein the video decoder at least performs picture level processing" limitation of claims 1 and 8, the Applicant respectfully traverses the rejection; however, in an effort to advance prosecution in the application, the Applicant has amended claims 1 and 8 to remove the limitation. Therefore, the rejection is moot and the Applicant respectfully requests that the rejections of Applicant's claims 1-14 and 16-18 under 35 U.S.C. § 112, first paragraph, be withdrawn.

Rejections Under 35 U.S.C. §102(e) - MacInnis

Claims 1-14 and 16-18 were rejected under 35 U.S.C. §102(e) as being anticipated by MacInnis et al. (U.S. Pub. No. 2003/0185306, hereinafter "MacInnis"). Without acknowledging that MacInnis qualifies as prior art under 35 U.S.C. §102(e), the Applicant respectfully traverses the rejections for at least the following reasons.

With regard to the anticipation rejections, MPEP 2131 states, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). MPEP 2131 also states, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Regarding claim 1, the Applicant respectfully submits that the cited sections of MacInnis fail to teach, suggest, or disclose, for example, "a host processor for providing an indication to the video decoder indicating the particular encoding standard, wherein the video decoder for decoding the video data encoded with the particular standard is discrete from the host processor," as set forth in Applicant's independent claim 1.

The Office Action alleges that "MacInnis teaches, a system for decoding video data encoded with a particular standard, said system comprising: a video decoder for decoding the video data encoded with the particular standard, wherein the video decoder at least performs picture level processing (figs. 4a, elements 302 and 306...)." (Office Action, Page 4). The Applicant appreciates the Examiner's acknowledgement that MacInnis's core decoder processor 302 is part of MacInnis's video decoder 300. It is unclear from the Office Action, however, what the Examiner is alleging is a "host processor" in MacInnis. For example, the Office Action alleges that MacInnis's Figure 3 discloses a host processor discrete from the video decoder.

(Office Action, Page 4, 3rd Bullet Point). However, MacInnis's Figure 3 merely illustrates a high-level functional block diagram of the digital video decoding system 300 illustrated in MacInnis's Figure 4a.

Thus, if the Examiner is alleging that MacInnis's core decoder processor 302 is both part of the video decoder 300 and a host processor, the Applicant notes that the cited sections of MacInnis clearly cannot teach "a host processor for providing an indication to the video decoder indicating the particular encoding standard, **wherein the video decoder** for decoding the video data encoded with the particular standard **is discrete from the host processor**," as set forth in Applicant's independent claim 1. Alternatively, if the Examiner is alleging that MacInnis's core decoder processor 302 is a host processor discrete from MacInnis's video decoder 300, the Applicant notes that such allegation would be inconsistent with the Examiner's arguments (as discussed above) and the cited sections of MacInnis, which teaches "[t]he core processor 302 is the master of the decoding system 300. It controls the data flow of decoding processing. All video decode processing, except where otherwise noted, is performed in the core processor." (MacInnis, Paragraph [0040], Lines 1-4). Because the Office Action has failed to show "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference" as required for an anticipation rejection under MPEP 2131, the rejection of claim 1 under 35 U.S.C. § 102(e) cannot be maintained.

Therefore, for at least the above stated reasons, Applicant respectfully submits that the cited sections of the MacInnis reference fails to teach, suggest, or disclose Applicant's invention as set forth in claim 1. The Applicant believes that claim 1 is allowable over MacInnis. Applicant respectfully submits that claim 1 is an independent claim, and that claims 2-7 depend either directly or indirectly from independent claim 1. Because claims 2-7 depend from claim 1, Applicant respectfully submits that claims 2-7 are allowable over the MacInnis reference, as well. The Applicant respectfully requests, therefore, that the rejection of claims 1-7 under 35 U.S.C. §102(e), be withdrawn.

Regarding claim 8, the Applicant respectfully submits that the cited sections of MacInnis fail to teach, suggest, or disclose, for example, "receiving an indication from a host processor by a video decoder indicating the particular encoding standard, wherein the video decoder is discrete from the host processor," as set forth in Applicant's independent claim 8.

As discussed above, the Applicant appreciates the Examiner's acknowledgement that MacInnis's core decoder processor 302 is part of MacInnis's video decoder 300. It is unclear from the Office Action, however, what the Examiner is alleging is a "host processor" in MacInnis. If the Examiner is alleging that MacInnis's core decoder processor 302 is both part of the video decoder 300 and a host processor, the Applicant notes that the cited sections of MacInnis clearly cannot teach "receiving an indication from a host processor by a video decoder indicating the particular encoding standard, **wherein the video decoder is discrete from the host processor**," as set forth in Applicant's independent claim 8. Alternatively, if the Examiner is alleging that MacInnis's core decoder processor 302 is a host processor discrete from MacInnis's video decoder 300, the Applicant notes that such allegation would be inconsistent with the Examiner's arguments (as discussed above) and the cited sections of MacInnis, which teaches "[t]he core processor 302 is the master of the decoding system 300. It controls the data flow of decoding processing. All video decode processing, except where otherwise noted, is performed in the core processor." (MacInnis, Paragraph [0040], Lines 1-4). Because the Office Action has failed to show "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference" as required for an anticipation rejection under MPEP 2131, the rejection of claim 8 under 35 U.S.C. § 102(e) cannot be maintained.

Therefore, for at least the above stated reasons, Applicant respectfully submits that the cited sections of the MacInnis reference fails to teach, suggest, or disclose Applicant's invention as set forth in claim 8. The Applicant believes that claim 8 is allowable over MacInnis. Applicant respectfully submits that claim 8 is an independent claim, and that claims 9-13 depend either directly or indirectly from independent claim 8. Because claims 9-13 depend from claim

8, Applicant respectfully submits that claims 9-13 are allowable over the MacInnis reference, as well. The Applicant respectfully requests, therefore, that the rejection of claims 8-13 under 35 U.S.C. §102(e), be withdrawn.

Regarding claim 14, the Applicant respectfully submits that MacInnis fails to teach, suggest, or disclose, for example, "wherein the processor loads the code memory after receiving an indication from a discrete host processor indicating the particular encoding standard," as set forth in Applicant's independent claim 14.

As discussed above, the Applicant appreciates the Examiner's acknowledgement that MacInnis's core decoder processor 302 is part of MacInnis's video decoder 300. It is unclear from the Office Action, however, what the Examiner is alleging is a "host processor" in MacInnis. If the Examiner is alleging that MacInnis's core decoder processor 302 is both part of the video decoder 300 and a host processor, the Applicant notes that the cited sections of MacInnis clearly cannot teach "wherein the processor loads the code memory after receiving an indication from **a discrete host processor** indicating the particular encoding standard," as set forth in Applicant's independent claim 14. Alternatively, if the Examiner is alleging that MacInnis's core decoder processor 302 is a host processor discrete from MacInnis's video decoder 300, the Applicant notes that such allegation would be inconsistent with the Examiner's arguments (as discussed above) and the cited sections of MacInnis, which teaches "[t]he core processor 302 is the master of the decoding system 300. It controls the data flow of decoding processing. All video decode processing, except where otherwise noted, is performed in the core processor." (MacInnis, Paragraph [0040], Lines 1-4). Because the Office Action has failed to show "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference" as required for an anticipation rejection under MPEP 2131, the rejection of claim 14 under 35 U.S.C. § 102(e) cannot be maintained.

Therefore, for at least the above stated reasons, Applicant respectfully submits that the cited sections of the MacInnis reference fail to teach, suggest, or disclose Applicant's invention as set forth in claim 14. The Applicant believes that claim 14 is allowable over MacInnis. Applicant respectfully submits that claim 14 is an independent claim, and that claims 16-18 depend either directly or indirectly from independent claim 14. Because claims 16-18 depend from claim 14, Applicant respectfully submits that claims 16-18 are allowable over the MacInnis reference, as well. The Applicant respectfully requests, therefore, that the rejection of claims 14, 16-18 under 35 U.S.C. §102(e), be withdrawn.

New Claims

The present application adds new claims 21-23. New dependent claims 21, 22 and 23 depend from claims 1, 8 and 14, respectively. Thus, the Applicant submits that, for at least the reasons discussed previously with regard to claims 1, 8 and 14, new claims 21-23 are allowable over MacInnis as well. Additionally, the Applicant submits that each of claims 21-23 is independently allowable.

Final Matters

The Office Action makes various statements regarding claims 1-14 and 16-18, 35 U.S.C. § 112, first paragraph, 35 U.S.C. § 102(e), the MacInnis reference, etc. that are now moot in view of the above amendments and/or arguments. Thus, the Applicant will not address all of such statements at the present time. However, the Applicant expressly reserves the right to challenge such statements in the future should the need arise (e.g., if such statements should become relevant by appearing in a rejection of any current or future claim).

Applicant reserves the right to argue additional reasons supporting the allowability of claims 1-14, 16-18 and 21-23 should the need arise in the future.

CONCLUSION

Applicant respectfully submits that all of claims 1-14, 16-18 and 21-23 are in condition for allowance, and requests that the application be passed to issue.

Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the telephone number listed below.

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Dated: May 29, 2009

Respectfully submitted,

/Philip Henry Sheridan/
Philip Henry Sheridan
Reg. No. 59,918

McAndrews, Held & Malloy, Ltd.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
(T) 312 775 8000
(F) 312 775 8100